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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/560,646	12/13/2005	Takefumi Nishimuta	5000-5292	6908

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EXAMINER	
HU, SHOUXIANG	
ART UNIT	PAPER NUMBER
2811	

NOTIFICATION DATE	DELIVERY MODE
02/26/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/560,646	NISHIMUTA ET AL.	
	Examiner	Art Unit	
	Shouxiang Hu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/14/07; 12/13/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 4, 7 and 8 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claims 4 and 7 recite the combination of subject matters that the limiter circuit comprises two transistors, including a p-channel MIS field-effect transistor (p-MIS) and an n-channel MIS field-effect transistor (n-MIS); and that channel widths of the two transistors are set such that the current drive capability of the p-channel MIS field-effect transistor can be substantially equal to current drive capability of the n-channel MIS field-effect transistor. However, the disclosure lacks an adequate description regarding which two of the transistors in the limiter circuit of the instant invention (as shown in Fig. 5) are readable as the recited two transistors (the n-MIS and the p-MIS). The disclosure lacks an identification of the two transistors with such matched performance capability in the disclosed sole limiter circuit shown in Fig. 5.

Claim 8 recite the subject matters that the limiter circuit comprises a CMOS, including a p-channel MIS field-effect transistor (p-MIS) and an n-channel MIS field-effect transistor (n-MIS). However, the disclosure lacks an adequate description regarding which two of the transistors in the limiter circuit of the instant invention as shown in Fig. 5 form the recited CMOS (the n-MIS and the p-MIS). The disclosure lacks an identification of the two transistors in the disclosed sole limiter circuit shown in Fig. 5, given that the two transistors in a CMOS commonly share a same gate line in the circuit.

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1 and 6 each recite the subject matters of a drain and a source are formed on both sides enclosing the gate insulating film of the projecting portion; but it appears to be incomprehensible, as it is not clear what is the subject that definitely enclosing the recited gate insulating film, given that the word of "enclose" may mean to cover from all directions; and/or where definitely the recited source and/or drain is/are formed; and/or how the recited source and drain could enclose the recited gate insulating film, given that they each have to be formed inside the projecting portion and directly contact with the channel region.

Claims 1 and 6 each recite the subject matters that a projecting portion is formed by a silicon substrate; but it is not clear how and/or in what sense the recited projecting portion could be formed "by" the recited silicon substrate, given that the recited projecting portion can only be formed by relevant process steps in the instant invention, and/or that the projecting portion is in fact located on the substrate in the instant invention.

Claims 1 and 6 each recite the term of "the silicon surface", but it lacks a sufficient antecedent basis in the claims.

Claim 3 recites the subject matters of the drain and source are formed on the projecting portion enclosing the gate and in left and right areas of the projecting portion of the silicon substrate. But it fails to clarify: what is the subject that definitely enclosing the recited gate, given that the word of "enclose" may mean to cover from all directions; and/or where definitely the recited source and/or drain is/are formed; and/or how the left and right areas are definitely defined, given that viewing from different directions may lead to different identifications about left and right.

Claims 4 and 5 define additional transistors, but fail to clarify their relationship with the transistor(s) already recited in claim 1. Are they same or different entities?

Claim 6 recites the terms of "a circuit" and "a limiter circuit", but fails to clarify their relationship, and/or which is within which.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-8, insofar as being in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Toyoshima (Toyoshima et al., US 2003/0235058) in view of Hieda (US 2002/0011612).

Toyoshima discloses a limiter circuit (Fig. 1), which is naturally formed on a semiconductor integrated circuit substrate, comprising:

a differential amplification circuit (Fig. 8) comprising an MIS field-effect transistor (MISFET; such as 1405 or 1406) among the n-type MISFETs (1405-1407) and the p-type MISFET (1401-1404).

Although Toyoshima does not expressly disclose that the transistor can be formed of a tri-gated transistor that has a projecting portion, one of ordinary skill in the art would readily recognize that such tri-gated transistor can be desirable formed so as to reduce the device size with improved performance, as evidenced in Hieda. Hieda teaches to form such tri-gated transistor (Figs. 1-76, particularly see the one shown in Figs. 2-11; also see [0543]), comprising: a projecting portion (13) formed by/on a silicon substrate (including 10) having a first crystal surface (such as (100), see [0175]) as a primary surface and the projecting portion naturally has a second crystal surface as a side surface; a gate insulating film (18); a gate (16) formed on the gate insulating film;

and, drain and source (17 and/or 28) formed in and/or on the projecting portion on both sides of the channel region and/or on both sides of the gate insulating film, wherein the gate naturally includes the top gate portion and the two side gate portions (i.e., a tri-gated structure).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the tri-gated MOS field effect transistor of Hieda into the device of Toyoshima, so that a limiter circuit device with reduced size and/or with improved performance would be obtained.

Furthermore, it is noted that the limitations of "terminated hydrogen on the silicon surface is removed in plasma atmosphere of an inert gas" and "at a temperature at or lower than about 550°C in the plasma atmosphere" recited in the claims are process limitations; but these would not carry patentable weight in the claims drawing to a structure, because distinct structure is not necessarily produced. In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985).

Regarding claim 2, it is noted that, in the MIS field effect transistor of Hieda, a channel is naturally formed on the first crystal surface of the top surface and the second crystal surface of the side surface of the projecting portion, and a channel width of the MIS field-effect transistor is naturally at least a total of channel widths on the top surface and the side surface.

Regarding claim 3, it is noted that, in the MIS field effect transistor of Hieda, the projecting portion has the top surface naturally comprising a silicon surface (100), given that the substrate has such orientation. And, it is noted that it is well known in the

art the side surface can be desirably oriented along (110) for achieving improved performance for the side channel/channels, as readily evidenced in the prior art such as Lee (US 2004/0150029; see [0038]).

Regarding claims 4 and 7, it is noted that, insofar s being in compliance with 35 U.S.C. 112, it is well known that the current drive capability of the individual transistors is directly correlated with the gate width; and that each gate width of two transistors paired together is an art-recognized result-oriented parameter of importance, subject to experimentation and optimization; and that it is art known that the complementarily paired transistors can desirably have substantially same drive performance, as further evidenced in Hieda (see Figs. 48-54; also see [0418] through [0420]). Accordingly, it would be well within the ordinary skill in the art to form the above collectively taught device with the gate width of each of the complementarily paired transistors therein being designed so as to achieve the desired substantially same drive performance in the paired transistors therein.

Regarding claim 5, it is noted that the first and second MIS field-effect transistors (1405 and 1406) in Toyoshima naturally form a differential amplification circuit for receiving a signal at a gate; and a third MIS field-effect transistor (1047) therein forms a constant current circuit commonly connected to a source or a drain of the first and second MIS field-effect transistors. Furthermore, it is noted that, the recited limitation of "for receiving an FM-modulated signal" is an intended use limitation. However, recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the

claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In this case, the limiter of Toyoshima is for the use of SRAM, it can naturally capable of receiving FM-modulated signal to the gate, regardless whatever its response may be.

Regarding claim 8, it is noted that, insofar as being in compliance with 35 U.S.C. 112, at least the p-channel MIS field-effect transistor (1401) and the n-channel MIS field-effect transistor (1405) in the limiter circuit of Toyoshima can be regarded as a CMOS, since that are complementary to each other and connected in series.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. References B and C are cited as being related to a limiter circuit; and D to a Fin-MOSFET structure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is 571-272-1654. The examiner can normally be reached on Monday through Friday, 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Shouxiang Hu/
Primary Examiner, Art Unit 2811
February 15, 2008